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## P a t e n t   c l a i m s

(Amended December 15, 2004)

1.     An arrangement for interconnection of two or more  
printed circuit board's communicating with each other over  
5     a time division multiplex data bus, each including a number  
of loads transferring data in both receive and transmit  
direction,  
c h a r a c t e r i z e d   i n

10     a local time division multiplex data bus in each  
printed circuit board to which the associated number  
of loads are connected,

15     an intermediate Central Processing Unit controlled  
logic in each direction connecting a local time  
division multiplex data bus to a global time division  
multiplex data bus, which logic includes a First-In-  
First-Out buffer through which synchronous data from  
the local or global data bus is being written in and  
read out to the local or global data bus introducing a  
phase difference providing a total delay for any data  
20     travelling from a local time division multiplex bus to  
the global time division multiplex data bus and back  
to a local time division multiplex data bus being of a  
controllable dimension equal to an integer number of  
data frames.

25     2.     Arrangement as defined in claim 1,  
c h a r a c t e r i z e d   i n that the global time  
division multiplex data bus is a back plane time division  
multiplex data bus, and said arrangement is implemented in  
a circuit switched node.

30     3.     Arrangement as defined in claims 2,  
c h a r a c t e r i z e d   i n     that the logic further  
includes a first and a second time slot counter, the first

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counter addressing a first data location in the First-In-First-Out buffer into which, in case of receive direction, time slot data from a local time division multiplex data bus is to be written, or out of which, in case of transmit  
5 direction, time slot data to a local time division multiplex bus is to be read, the second counter addressing a second data location in the First-In-First-Out buffer into which, in case of transmit direction, time slot data from the global time division multiplex bus is to be  
10 written, or out of which, in case of receive direction, time slot data to the global time division multiplex bus is to be read, wherein the phase difference between the first and the second time slot counter represents a preferred part of said total delay caused by the logic of the  
15 respective direction.

4. Arrangement as defined in claim 3,  
c h a r a c t e r i z e d i n that the first counter is incremented by a first clock (TDM\_CLK LOCAL) corresponding to the current local time division multiplex data bus and  
20 initialised by a first frame synchronisation signal (FSYNC LOCAL) indicating the start of each frame in the current local time division multiplex data bus, the second counter is incremented by a second clock (TDM\_CLK EXTERN) corresponding to the global time division multiplex data  
25 bus and initialised by a second frame synchronisation signal (FSYNC EXTERN) indicating the start of each frame in the global time division multiplex data bus.

5. Arrangement as defined in claim 4,  
c h a r a c t e r i z e d i n that the first clock and  
30 frame synchronisation signal is derived from the second clock and frame synchronisation signal, adapted to provide said preferred part of said total delay caused by the logic of the respective direction.

6. Arrangement as defined in one of the claims 3 - 5,  
35 c h a r a c t e r i z e d i n that the logic further

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includes a table including one bit per data location in the First-In-First-Out buffer, wherein, in case of transmit direction, if a first logic value is assigned to the data location addressed by the first counter, reading of the content in that data location to the certain local time division multiplex data bus is enabled, in contrast to a second logic value in which case reading is disabled, and in case of receive direction, if a first logic value is assigned to the data location addressed by the second counter, reading of the content in that data location to the global time division multiplex data bus is enabled, in contrast to a second logic value in which case reading is disabled.

7. Arrangement as defined in one of the claims 3 - 6, characterized in that the preferred part of said total delay caused by the logic of the receive direction is the duration of one frame minus the preferred part of said total delay caused by the logic of the transmit direction.

8. Arrangement as defined in claim 7, characterized in that the preferred part of said total delay caused by the logic of the transmit direction is the duration of 8 or 16 time slots.

9. Arrangement as defined in one of the preceding claims, characterized in that the circuit switched node is a Base Station Controller (BSC) or a switch in any circuit switched enabled data or telecommunication network.